NATIONAL TRANSPORTATION SAFETY BOARD

OFFICE OF AVIATION SAFETY
WASHINGTON, D.C. 20594

June 2, 2017

FIELD NOTES

NTSB ID No.: CEN17FA183 (CEN17MA183)

A: ACCIDENT

Location:	Teterboro, New Jersey
Date:	May 15, 2017
Time:	1529 eastern daylight time
Aircraft:	Gates Learjet 35A, N452DA, Trans-Pacific Jets

B: GROUP

Investigator:	Gordon J. Hookey National Transportation Safety Board Washington, D.C.
Member:	David Studtman Honeywell Phoenix, Arizona

C: SUMMARY

On May 15, 2017 at 1529 eastern daylight time, a Gates Learjet 35A, N452DA, operated by Trans-Pacific Jets, departed controlled flight while on a circling approach to runway 1 at the Teterboro Airport (TEB), Teterboro, New Jersey, and impacted a commercial building and parking lot. The captain and first officer died; no one on the ground was injured. The airplane was destroyed by impact forces and postcrash fire. The airplane was registered to the A&C Big Sky Aviation LLC and operated by Trans-Pacific Air Charter LLC under the provisions of 14 Code of Federal Regulations Part 91 as a positioning flight. Visual meteorological conditions prevailed, and an instrument flight rules flight plan was filed. The flight departed from the Philadelphia International Airport, Philadelphia, Pennsylvania, at about 1504 and was destined for TEB.

The accident airplane was equipped with two Honeywell TFE731 turbofan engines that each have a digital electronic engine control (DEEC) installed. The DEECs have a memory chip

that has non-volatile memory (NVM) that can retain airplane and engine operational data. On June 2, 2017, the memory chips as well as the DEEC circuit boards that the memory chips had been installed on[1] were taken to the Honeywell facility in Tucson, Arizona to attempt to down load the NVM data in the presence of investigators from the NTSB and Honeywell Product Integrity office. The NVM could not be downloaded from either DEEC's memory chip. One of the DEEC's memory chip had apparent damage to the internal electrical connections. The other DEEC's chip had many connecting pins missing and broken as well as having the cover separated from the chip that exposed visible damage to the internal electrical connections.

D: DETAILS OF INVESTIGATION

1. General

The two DEEC circuit boards along with their respective NVM chips arrived at the Honeywell Tucson, Arizona facility sealed in a box. (Photo No. 1) The box had been opened the day before by the NTSB investigator at the Honeywell Phoenix, Arizona facility to confirm the circuit boards and memory chips were in the box. Upon confirmation the circuit boards and memory chips were in the box, the box was immediately resealed for transport to Tucson.

Photo No. 1: Sealed box containing the two DEEC boards. (Honeywell)

2. Circuit board and chip A

The circuit board that was identified as "A" was sealed in a plastic bag along with the NVM chip that had been removed from the board and was contained in a small box. The board was partially burned on one end. (Photo No. 2) The center part of the board was missing the

[1] The memory chips had been removed from their respective circuit boards at the NTSB Recorder Laboratory prior to being shipped to Honeywell, Phoenix, Arizona.

resin coating exposing the fiberglass matting. (Photo No. 3) The underside of the board had metal slag adhered to it. (Photo No. 4)

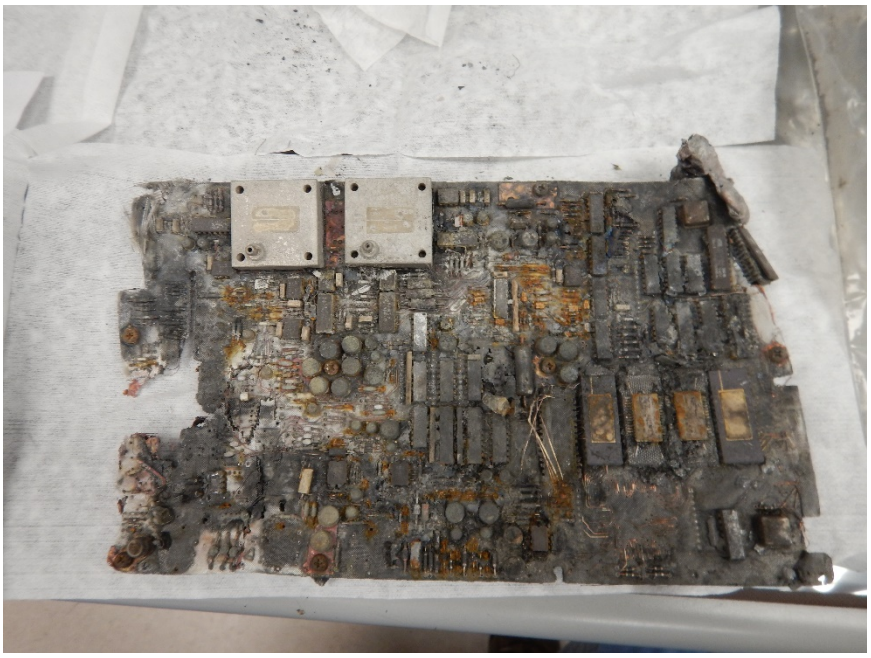


Photo No. 2: Board "A" partially burned on one end. (Honeywell)

Photo No. 3: Close up view of board "A" showing exposed fiberglass matting. (Honeywell)

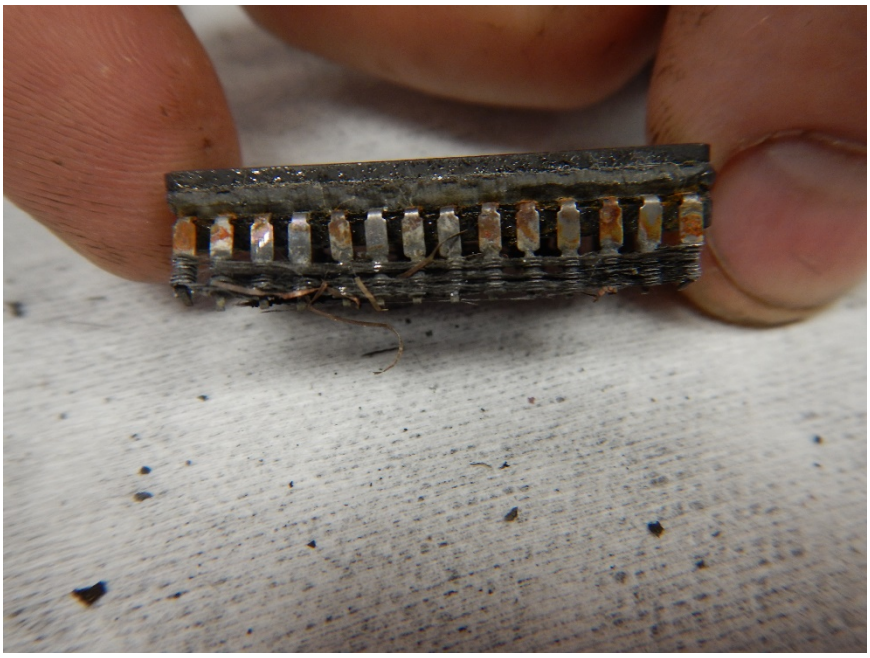
Photo No. 4: Underside of board "A" showing metal slag. (Honeywell)

The memory chip was intact and the cover was in place. The cover and the underside of the chip had a mottled appearance and there was no legible writing on either side. (Photos Nos 5 and 6) Although the cover was in place, it was partially lifted at one end. (Photo No. 7) All of the pins were in place on the chip, but there were many pins that were bent slightly. (Refer to Photo No. 6) The pins had a lot of layered debris, consistent with the layers of material from the fiberglass board. (Photo No. 8)

Photo No. 5: Top of chip. (Honeywell)

Photo No. 6: Underside of chip also showing the bent pins.(Honeywell)

Photo No. 7: Side view of chip showing partially lifted cover. (Honeywell)



(Photo No. 8: Close up view of pins showing layers of debris. (Honeywell)

After the pins were cleaned (Photo No. 9), the chip was positioned into the receptacle of a data reader. Several attempts were made to read the data, but all resulted in indications of a continuity fail message or a message that indicated there was no data stored in the NVM. A digital multimeter was used to check the continuity between the chip's two power pins, Nos. 14 and 28, that indicated there was no continuity. When the multimeter was used to check the continuity between the power pins on an exemplar memory chip, it showed that there was continuity between the two pins.

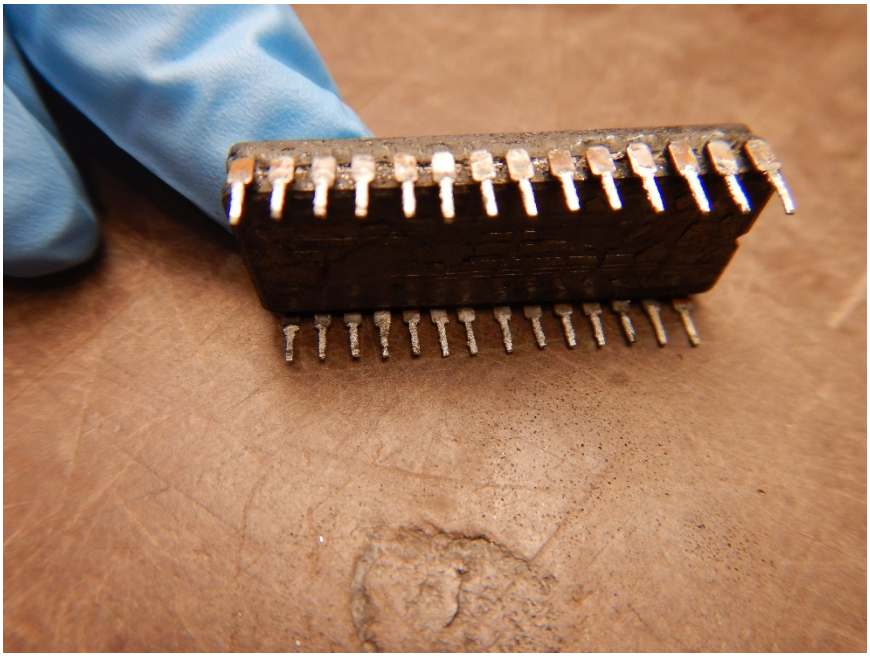


Photo No. 9: Close up view of pins after they had been cleaned. (Honeywell)

3. Board B

The board that was identified as "B" was sealed in a plastic bag along with the NVM chip that had been removed from the board and was contained in a small box. The board was intact. (Photo No. 10)

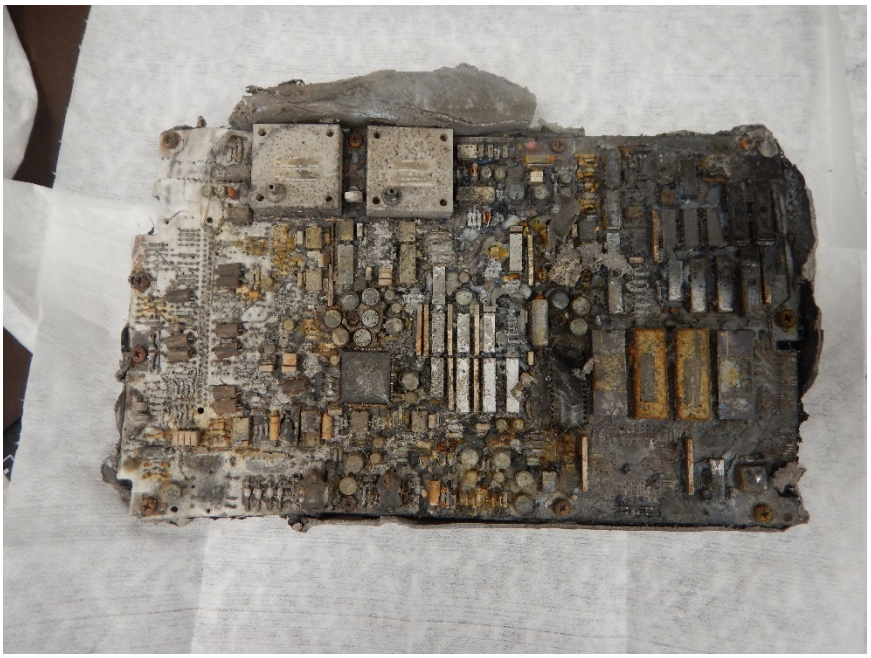


Photo No. 10: View of board "B" showing it was intact. (Honeywell)

The body of the chip was intact, but the cover had separated from the body exposing the die, the leads to the pins, and the fly wires. (Photo No. 11) Most of the fly wires between the pins and the die were missing. Of the 28 pins on the chip, 17 were broken away and missing from the chip. Of the 11 pins that remained on the chip, 9 were on one side and 2 on the other side. (Photo No. 12) The ends of most of the missing pins could be felt or seen still in the board. The die appeared to be intact. (Photo No. 13)

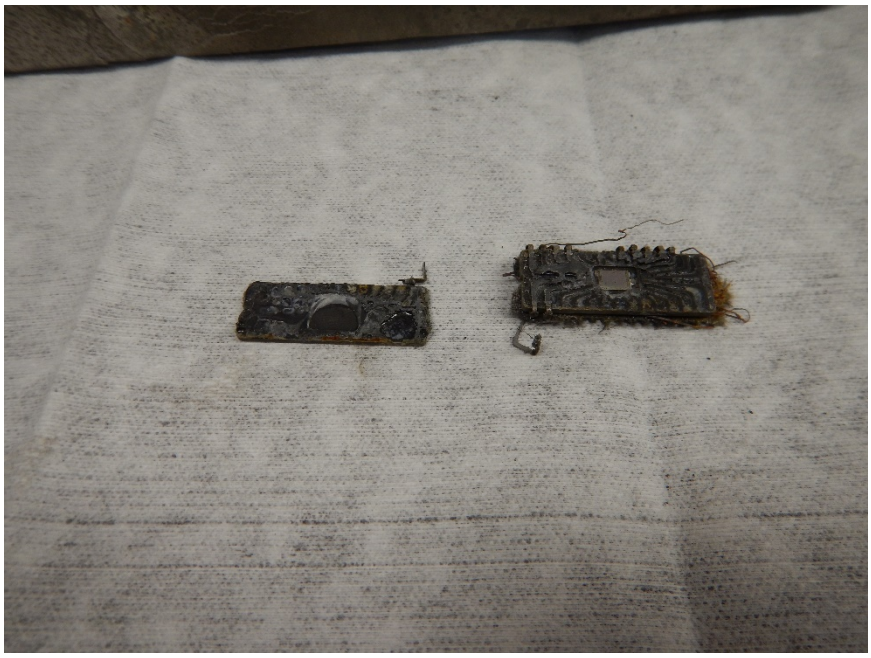


Photo No. 11: Chip showing the cover had separated exposing the inside: (Honeywell)

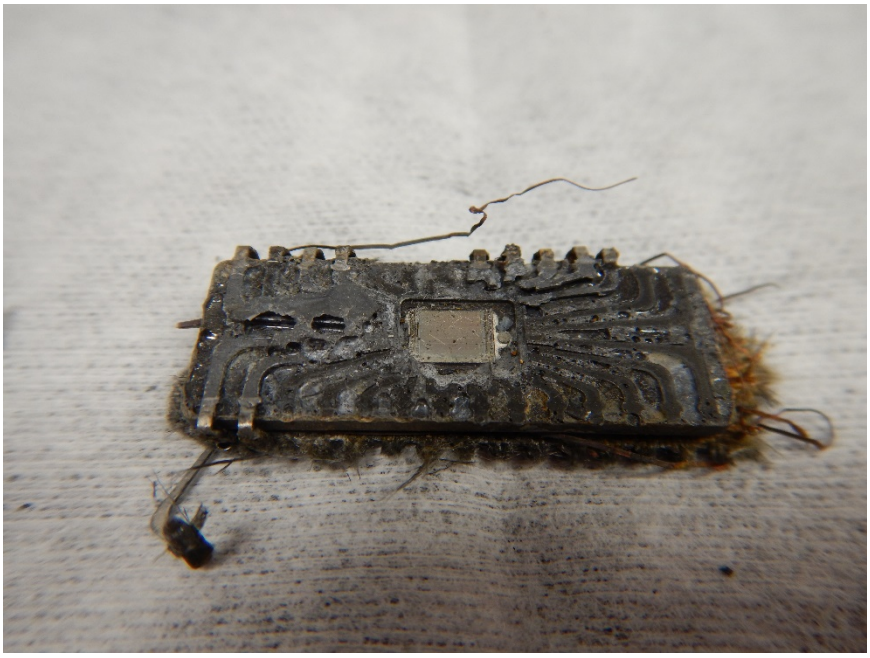


Photo No. 12: Close up of chip showing most of the fly wires were missing. (Honeywell)

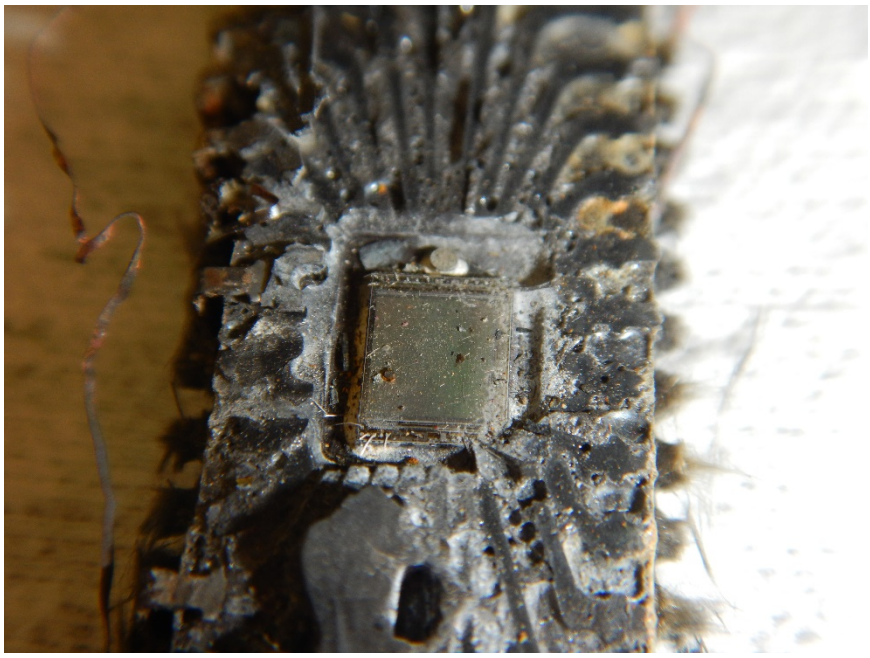


Photo No. 13: Close up of die showing that it was intact. (Honeywell)

Markings that were noted on the underside of the chip and compared to an exemplar memory chip indicated the chip had been manufactured by Atmel. (Photos Nos. 14, 15, and 16) According to Honeywell, Atmel, which is based in San Jose, California, was the designated vendor for the memory chips in the DEECs that were installed on the accident engines.

Photo No. 14: Markings on underside of memory chip from accident DEEC. (Honeywell)

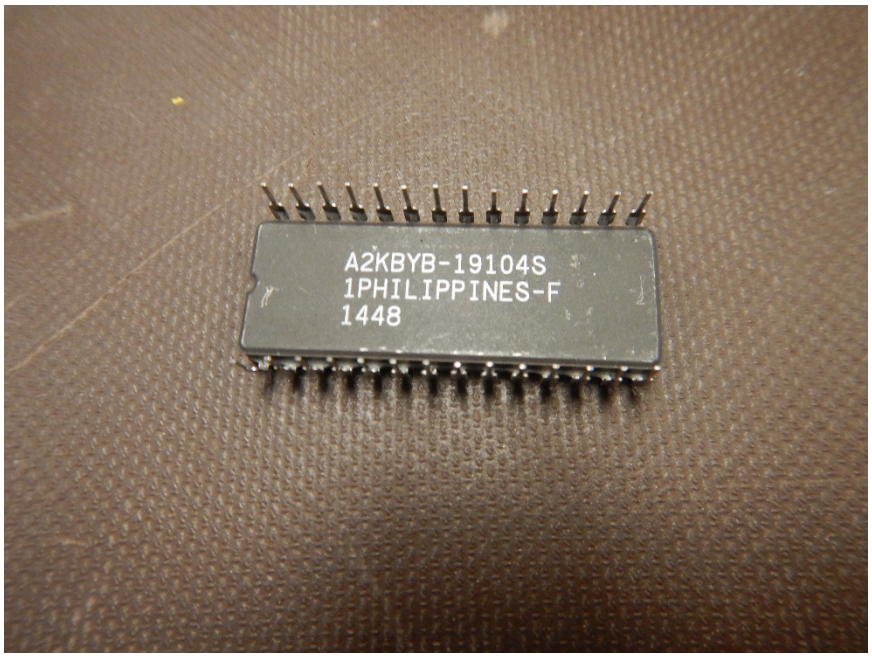


Photo No. 15: Markings on underside of exemplar memory chip. (Honeywell)

Photo No. 16: Markings on top of exemplar memory chip. (Honeywell)